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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/749,575

12/31/2003

Peter Capofreddi

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LADAS & PARRY

5670 WILSHIRE BOULEVARD, SUITE 2100
LOS ANGELES, CA 90036-5679

EXAMINER

PHU, PHUONG M

ART UNIT

PAPER NUMBER

2611

MAIL DATE

DELIVERY MODE

06/05/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/749,575

Applicant(s)

CAPOFREDDI, PETER

Examiner

Phuong Phu

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-20 is/are allowed.
- 6) ☒ Claim(s) 1, 4 and 5 is/are rejected.
- 7) ☒ Claim(s) 2, 3 and 6-10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/12/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Melanson (6,727,832).

-Regarding to claim 1, Melanson discloses a method comprising:

procedure (102) (see figure 1A) of receiving a multiple bit digital input signal in a signal band outputted from (101) (see col. 3, lines 28-66);

procedure (102) of providing a quantized representation of said multiple bit digital input signal (see col. 3, lines 28-66);

procedure (comprising (210a, 211a) (see figure 2E) of providing a first-order shaper circuit ($1/(1-z^{-1})$) for shaping quantization noise (see col. 1, lines 15-31, col. 6, line 64 to col. 7, line 10);

procedure (comprising (210a) (see figure 2C and 2D) of providing at least one higher-order shaper circuit which inherently filters possible NLISI and other undesired interferers lying outside bandwidth of filter (210a), (said filtering considered here equivalent with the limitation “spectrally shape NLISI”); and

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procedure (214, 215, 220) (see figure 2C) of changing said quantized representation based on said first order shaper circuit and said at least one higher-order shaper circuit (see col. 6, line 29 to col. 7, line 59), thereby inherently reducing possible NLISI energy level present in said signal band lying outside bandwidth of filter (102).

-Regarding to claim 4, Melanson teaches that said quantization representation is a single-bit representation (see col. 7, lines 49-51).

3. Claims 1, 4 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Melanson et al (6,822,594).

-Regarding to claim 1, Melanson et al discloses a method comprising:

procedure (202) (see figure 2) of receiving a multiple bit digital input signal (x_i) in a signal band outputted from (214) (see col. 7, lines 34-38);

procedure (202) of providing a quantized representation of said multiple bit digital input signal (see col. 7, lines 25-48);

procedure (206) (see figure 2) of providing a first-order shaper circuit for shaping/suppressing possible quantization noise lying out of band (see col. 1, lines 59-64, col. 4, line 35 to col. 5, line 10);

procedure (204) (see figure 2) of providing at least one higher-order shaper circuit which inherently filters possible NLISI and other undesired interferers lying out of band (see col. 1, lines 59-64, col. 4, line 35 to col. 5, line 10), (said filtering considered here equivalent with the limitation "spectrally shape NLISI"); and

procedure (208) (see figure 2) of changing said quantized representation based on said first order shaper circuit and said at least one higher-order shaper circuit (see col. 5, lines 10-66),

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thereby inherently reducing possible NLISI energy level present in said signal band lying out of band.

-Regarding to claim 4, Melanson et al teaches that said quantization representation is a single-bit representation (see col. 5, lines 10-15).

-Regarding to claim 5, as similarly applied to claims 1 and 4, set forth above and herein incorporated, Melanson et al discloses an oversampling multi-bit digital to analog converter (comprising (200) (see figure 2)) for converting a multi-bit converter digital input (x_i) to an analog converter output, comprising:

a digital signal processor (202) that spectrally shapes quantization noise using delta-sigma modulation, the digital signal processor comprising a first order shaper circuit (206) for shaping quantization noise;

wherein the digital signal processor comprises a multiport quantizer (208) (see figure 2) converting a plurality of multi-bit multiport inputs to a single-bit multiport output, and wherein the digital signal processor comprises at least one higher-order shaper circuit (204) (see figure 2) to spectrally shape possible nonlinear intersymbol interference (NLISI).

Melanson further teaches an analog filter ("analog low pass filter") included in (218) (see figure 2) of receiving the 1-bit output data from (202) (see col. 7, lines 40-49); and a unitary digital-to-analog converter "DAC" (see col. 1, lines 47-54) (inherently included in (218)) connected between the digital signal processor (202) and the analog filter for converting the 1-bit output data to an analog input for the input of the analog filter.

Allowable Subject Matter

4. Claims 11-20 are allowed.

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5. Claims 2, 3 and 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu

**PHUONG PHU
PRIMARY EXAMINER**

Phuong Phu
Primary Examiner
Art Unit 2611

Phuong Phu
05/31/07